(19) Japan Patent Office (JP)

(12) Gazette of Patents (A)

(11) Unexamined Patent Application Number: 7-128685

(43) Date of Publication: May 19, 1995

(51) Int. Cl.^{6}:		Identification Symbol:	Domestic Classification Number:		F1
G 02 F	1/136	500			
	1/133	550			
H 01 L	29/786				
			9056-4M	H01L 29/78	311 A

Request for Examination: Not yet made

Number of Claims: 4 (Number of Pages: 6)

---

(21) Application Number: *Tokuganhei* 5-275732

(22) Date of Application: November 4, 1995

(71) Applicant: 000002369

SEIKO EPSON Co., Ltd.,

4-1, 2-chome, Nishishinjyuku, Shinjyu-ku, Tokyo

(72) Inventor: Makoto MATSUO

c/o SEIKO EPSON Co., Ltd.

3-5, 3-chome, Owa, Suwa, Nagano

(74) Attorney: Kisaburo SUZUKI, Patent Attorney (and one other)

Japanese Unexamined Patent Publication No. 128685/1995 (*Tokukaihei* 7-128685)

A. <u>Relevance of the Above-identified Document</u>

The following is a partial English translation of exemplary portions of non-English language information that may be relevant to the issue of patentability of the claims of the present application.

[Title of the Invention]

Liquid Crystal Display Device

[Abstract]

[Object] The black matrix is provided on an active-matrix substrate to reduce crosstalk due to source line potential, and increase the pixel storage capacitance and aperture ratio of the panel.

[Constitution] On the active-matrix substrate, a light-shielding black matrix is formed between a pixel electrode layer and a source line layer via an interlayer insulating film. A specific potential is applied to the black matrix to shield the source lines. The black matrix forms a storage capacitance with the pixel electrode.

[Claims]

[Claim 1]

A liquid crystal display device that includes an active-matrix substrate, a counter substrate, disposed parallel to the active-matrix substrate, and liquid crystal

interposed between the active-matrix substrate and the counter substrate, wherein the active-matrix substrate includes: a plurality of source and gate lines; a thin-film transistor, which defines a grid formed by the source and gate lines and has a source and a gate that are connected to the data and gate lines; and a pixel electrode connected to a drain of the thin-film transistor,

wherein at least a majority of the source lines is covered with a wiring layer via an interlayer insulating film, and a specific potential is applied to the wiring layer, and wherein the wiring layer is covered with an interlayer insulating film B, and the pixel electrode is formed to partially overlap with the wiring layer, so as to allow the wiring layer to form a storage capacitance in an area of overlap with the pixel electrode.

[Claim 2]

The liquid crystal display device as set forth in claim 1, wherein the wiring layer is a black matrix for shielding light and having a window pattern shaped along the pixel electrode.

[Claim 3]

The liquid crystal display device as set forth in claim 1, wherein the interlayer insulating film B is formed of an oxidized film of the wiring layer.

[Claim 4]

The liquid crystal display device as set forth in claim

1, wherein the specific potential applied to the wiring layer is equal to a counter electrode potential.

[Detailed Description of the Invention]

[0001]

[Field of the Invention]

The present invention relates to a structure of an active-matrix substrate for liquid crystal display devices.

[0002]

[Prior Art]

In a typical structure of liquid crystal display devices, liquid crystal is sealed between a pair of transparent substrates, wherein one of the transparent substrate is structured such that pixel regions are defined by a grid layout of data lines for supplying image signals and gate lines for sending scanning signals, and wherein the other transparent substrate has a common electrode. In this structure, a potential applied across the common electrode and a pixel electrode in each pixel region is controlled to change the alignment state of liquid crystal in each pixel region. In a liquid crystal display device of such a structure, a light-shielding black matrix is formed in one of the transparent substrates in order to improve accuracy of display at each pixel. Specifically, the black matrix is provided in regions of the transparent substrate with the common electrode, corresponding to boundary regions between the pixel regions. The two substrates are

mated so that the black matrix coincides with the boundary region between the pixel regions. Here, any misregistration between the black matrix and the boundary regions formed between the pixel regions deteriorates display quality. As a countermeasure, the black matrix has an extra margin in width to prevent such misregistration. However, providing an extra margin for the width of the black matrix is problematic in that it reduces the aperture ratio of the pixel regions (the proportion of area where display can be performed), with the result that display quality suffers. In view of such a problem, it has been proposed to form the black matrix on the transparent substrate provided with the matrix array. This is intended to prevent misregistration of the black matrix with the boundary regions between the pixel regions, and to provide a minimum required width for the black matrix.

[0003]

Figure 4 is a plan view illustrating one of the pixel regions of the matrix array provided with the black matrix. Figure 5 is a cross sectional view taken along line B-b. On a surface of a transparent substrate 9, source lines 2 and gate lines 1 are disposed in a grid pattern, and a black matrix light-shielding layer 8 of a window pattern is formed along transparent pixel electrodes 3. A thin film transistor 7 uses a polycrystalline silicon film 10 as an

active region, and a gate electrode 5 insulated by a gate insulating film 11 is connected to the gate lines 1. A source electrode 4 and a drain electrode 6 are connected to the source lines 2 and the pixel electrode 3, respectively, via through holes of the first interlayer insulating film 12. The light-shielding layer 8 is in a floating state by the presence of a second interlayer insulating film 13.

[0004]

[Problems to be Solved by the Invention]

In the active-matrix substrate of the foregoing structure, owning to the fact that the black matrix 8 is floating, capacitive coupling causes fluctuations in the pixel electrode potential, source line potential, or gate line potential. This easily causes 70 stalk1 in the horizontal and vertical directions. Further, since the pixel electrode is partially blocked by the light-shielding layer 8, the effective driving range of liquid crystal is small. In terms of alignment accuracy in the assembly of the panel, providing the black matrix on the active-matrix substrate provides a more margin. However, in terms of increasing the aperture ratio, the width of the black matrix needs to be reduced further. Referring to Figure 5, the source lines 2 and the pixel electrodes 3 are formed on the same plane, and therefore the distance between the two can be

1 The original text translates into "70 stalk", but this appears to be an error for "crosstalk."

reduced only to a certain extent. Figure 6 is a plan view illustrating a structure in which an interlayer insulating film is interposed between the source lines 2 and the pixel electrode 3, so as to decrease the distance between the two and thereby increase the aperture ratio. Figure 7 is a cross sectional view taken along line C-c of Figure 6. Referring to Figure 7, the second interlayer insulating film 13 covers the source lines 2, insulating the source lines 2 from the pixel electrodes 3. This enables the pixel electrode 3 to be positioned over the source lines 2, and thereby enables the width of the black matrix 8 formed on a third interlayer insulating film 14 to be reduced more than that shown in Figure 5. As a result, the aperture ratio is increased.

[0005]

However, a problem of this structure, attributed to the proximity of the source lines 2 and the pixel electrodes 3, is that changes in source line potential have adverse effects on the pixel potential due to the capacitive coupling. This causes crosstalk, or fluctuations of voltage-transmittance characteristics along the vertical direction of the panel. These problems are also caused in the structure shown in Figures 4 and 5 but are more apparent in the structure shown in Figures 6 and 7.

[0006]

Meanwhile, as the resolution is increased with a

narrower pitch, the liquid crystal alone is insufficient to provide enough storage capacitance for each pixel. As such, there is a need to provide load capacitance for each pixel. Currently, the load capacitance can be provided by a method in which a pixel auxiliary capacitance is formed using the gate line of the preceding stage, or by a method, known as a storage capacitance method, in which a new capacitor line is provided in a portion of the pixel regions. However, these methods greatly reduce the aperture ratio, and it has been difficult to provide enough storage capacitance.

[0007]

The present invention was made in view of the foregoing problems, and an object of the invention is to provide a high-resolution liquid crystal display device that does not cause crosstalk and provides a large aperture ratio, without sacrificing display quality or reliability.

[0008]

[Means to Solve the Problems]

In order to achieve the foregoing object, the invention provides a liquid crystal display device that includes an active-matrix substrate, a counter substrate, disposed parallel to the active-matrix substrate, and liquid crystal interposed between the active-matrix substrate and the counter substrate, wherein the active-matrix substrate includes: a plurality of source and

gate lines; a thin-film transistor, which defines a grid formed by the source and gate lines and has a source and a gate that are connected to the data and gate lines; and a pixel electrode connected to a drain of the thin-film transistor, wherein at least a majority of the source lines is covered with a wiring layer via an interlayer insulating film, and a specific potential is applied to the wiring layer, and wherein the wiring layer is covered with an interlayer insulating film B, and the pixel electrode is formed to partially overlap with the wiring layer, so as to allow the wiring layer to form a storage capacitance in an area of overlap with the pixel electrode.

[0009]

[Functions]

In a liquid crystal display device of the present invention, the black matrix is formed on the active-matrix substrate. In order to prevent adverse effects of pixel electrodes on a display, the black matrix has a specific potential and is provided beneath a pixel electrode layer via an insulating layer B. Further, in order to prevent crosstalk and fluctuation of voltage-transmittance characteristics along the vertical direction of the panel due to capacitive coupling between the pixel electrodes and the source lines, the black matrix shields the source lines via an insulating layer A. The insulating layer B on the black matrix forms a storage capacitance for each

pixel electrode.

[0010]

[EMBODIMENTS]

Referring to Figures 1 and 2, the following will describe one embodiment of the present invention.

[0011]

Figure 1 is a plan view illustrating a portion of a matrix array of a liquid crystal display device. Figure 2 is a cross sectional view of the matrix array taken along line A-a. In the descriptions below, constituting elements that are functionally equivalent to those described in conjunction with the liquid crystal display device shown in Figures 6 and 7 are given the same reference numerals.

[0012]

The following describes fabrication steps. First, a polycrystalline silicon thin film 10 is deposited on a transparent insulating substrate 9. After patterning, a gate insulating film 11 and a polycrystalline silicon thin film are deposited in this order. This is followed by doping with high-density impurities (phosphorous) to form N-type low resistant wirings. By patterning, gate electrodes 5 are formed. With the gate electrodes masked, source and drain regions 4 and 6 are formed by ion implantation. Next, a first interlayer insulating film 12 is deposited, and, after annealing, through holes are formed on the source region 4. Then, an Al alloy thin film is deposited, and

source lines are patterned. Thereafter, a second interlayer insulating film 13 (interlayer insulating film A) and a light shielding film are deposited, and a black matrix 8 is formed by patterning the light shielding film. The black matrix is formed so as to at least cover the source lines. If the black matrix is wider than the line width of the source lines by 2 μm or greater, leakage of electric field from the source lines can be relieved, which in turn reduces the component of capacitive coupling between the source lines and pixel electrodes. This reduces crosstalk and fluctuations of voltage-transmittance characteristics along the vertical direction. Next, a third interlayer insulating film (interlayer insulating film B) is formed. After forming through holes in the gate insulating film and the first through third interlayer insulating films, a transparent conductive film (ITO) is deposited and the pixel electrodes 3 are patterned. The result is the active-matrix substrate. The pixel electrodes 3 and the black matrix 8 are provided to partially overlap, so that the interlayer insulating film B can form a storage capacitance in the area of overlap. In order to provide enough storage capacitance with a small overlap area, it is preferable that the interlayer insulating film B be made of material with a large dielectric constant, or material which provides good insulation even when it is made into a thin film. Examples of the former include Ta_2O_5 and

Al_2O_3, and examples of the latter include SiO_2 and Si_3N_4. As a countermeasure against pinhole defects or dot defects, it is effective to form the interlayer insulating film B as an anodized film of the black matrix 8. Specifically, a β-TA metallization layer is deposited to 3000 Å as the black matrix 8. After freon dry etching, a Ta_2O_5 layer of 2000 Å thick is formed by applying a DC bias (anodization under applied voltage of 20 V) in an aqueous solution of diluted citric acid. The black matrix, which is a continuous pattern, is used in part as an anode around the substrate. Ta_2O_5 has a dielectric constant of about 25, and therefore can provide enough storage capacitance in the area of overlap of the pixel electrodes 3 and the black matrix. Insulation was sufficient as well. The anodized film is selectively formed only on the light shielding film patterns. This is advantageous in forming the through holes on the side of the pixel electrodes. The light shielding film may be made of Al alloy. Because Al alloy allows for anodization, the same effects can be obtained. Since the black matrix 8 is not floating, the black matrix 8 needs to be connected to a specific potential in regions around the panel. To this end, the black matrix 8 may be directly connected using anodization terminals, or may be connected to upper and lower contact terminals (area where the counter substrate and the active-matrix substrate are connected to each other via an upper and

lower conducting material for the purpose of applying a counter electrode potential) that are provided around the panel. In order to prevent deterioration of image quality caused by application of DC bias to the liquid crystal, it is desirable that the potential applied to the black matrix be a counter electrode potential.

[0013]

In this structure, line defects may be caused when shorting of the source lines 2, or the gate lines 1, and the black matrix 8 occurs in the pinholes of the first and second interlayer insulating films. The probability of such line defects is relatively low in the gate lines 1 because both the first and second interlayer insulating films are formed on the gate lines 1. However, the probability increases on the source lines where only the second interlayer insulating film is formed. In order to prevent such defects, the pin holes of the second interlayer insulating film on the source lines are closed by steam oxidation, prior to forming the light shielding film 8. It was equally effective to deposit the insulating film of SiO_2 or Ta_2O_5 before depositing the light shielding film 8.

[0014]

The counter substrate to be mated with the active-matrix substrate shown in Figures 1 and 2 may or may not be provided with a black matrix layer.

[0015]

The foregoing structure is also applicable to a panel in which a driving circuit is installed around the display area. In this case, a portion of the light shielding film can be used to shield not only the thin film transistors of the pixels but also the peripheral driving circuit. In this way, malfunctions caused by light can be prevented. Further, a portion of the light shielding film can also be used as a light-shielding corner frame, which may be optionally provided around the display area. The corner frame may be connected to a specific potential, or may be provided as a discrete pattern of a continuous layout.

[0016]

Figure 3 is a plan view representing another embodiment of the present invention. No cross sectional view is given here because it is essentially the same as that shown in Figure 2. In the structure illustrated in Figure 3, the black matrix 8 is divided along the gate lines. In this structure, the light shielding film 8 covers only portions of the source lines 2 and the pixel electrodes 3 where strong capacitive coupling occurs. This is intended to reduce the capacitance of the source lines and the light shielding film and thereby suppress defects. The same effects can also be obtained when the black matrix is divided along the source lines (not shown). The effect of preventing shorting as described above with reference to Figures 1 and 2 remains the same with the light shielding

film formed along the gate lines. However, if a group of even numbered lines and a group of odd numbered lines along the gate lines were connected to different potentials and were driven separately, it would be possible to suppress flicker or voltage-transmittance fluctuations in each odd numbered line.

[0017]

In order to prevent leakage of light between separated units of the light shielding film, the counter substrate needs to be provided with light shielding film patterns.

[0018]

For the shear purpose of preventing crosstalk caused by the capacitive coupling between the source lines and the pixels, it is only sufficient to use a transparent conductive film as the wiring layer to be the light shielding film 8. In this case, the counter substrate also needs to be provided with light shielding film patterns.

[0019]

The thin film transistor 7 shown in Figures 1 through 3 has the coplanar structure. However, the present invention is also applicable to the reverse staggered structure using amorphous silicon. Further, even though the present invention was described based on the mosaic arrangement, the invention is applicable to the delta arrangement as well.

[0020]

[Effects of the Invention]

As described above, a liquid crystal display device of the present invention has a structure in which a light-shielding black matrix is formed on an active-matrix substrate by being disposed between a pixel electrode layer and a source line layer via an interlayer insulating film. According to this structure, a specific potential is applied to the black matrix to shield source lines, and the black matrix forms a storage capacitance with the pixel electrodes. By virtue of this structure, the present invention exhibits the following effects.

[0021]

(1) Because the matrix array and the black matrix are formed on the surface of the transparent substrate, position registration of the black matrix with a boundary region between pixels is not necessary. Further, owning to the fact that the width of the black matrix does not require an extra margin, an aperture ratio can be increased.

[0022]

(2) Because the black matrix is held at a specific potential, there is no crosstalk either in the vertical direction or horizontal direction. This improves display quality. Further, reliability can be improved when the specific potential is the counter electrode potential.

[0023]

(3) Since the black matrix shields the source lines, it is possible to suppress crosstalk or fluctuation of voltage-transmittance characteristics along the vertical direction.

[0024]

(4) Since the storage capacitance is formed in an area of overlap of the pixel electrodes and the black matrix, uniform storage capacitance can be formed even when there is misregistration of pixel electrode patterns in horizontal and vertical directions. This prevents flicker and other undesirable effects. Further, pinhole defects can be prevented when the black matrix is formed of a Ta film and the interlayer insulating film B is formed by anodizing the Ta film into a TaO_5 layer. Further, in this case, a large storage capacitance can be formed over a small area, and the aperture ratio can be increased.

[0025]

(5) The structure allows the black matrix to be separated along the row or column direction. By driving the black matrix with application of a specific potential to each even numbered line, non-uniformity between lines can be relieved.

[0026]

(6) The structure allows a light-shielding corner frame to be formed around the display area, at the time of forming the black matrix and by using the same material.

[Brief Description of the Drawings]

[Figure 1]

A plan view illustrating a portion of a liquid crystal display device according to one embodiment of the present invention.

[Figure 2]

A cross sectional view taken along line A-a of Figure 1.

[Figure 3]

A plan view illustrating a portion of a liquid crystal display device according to another embodiment of the present invention.

[Figure 4]

A plan view illustrating a portion of a matrix array of a conventional liquid crystal display device.

[Figure 5]

A cross sectional view taken along line B-b of Figure 4.

[Figure 6]

A plan view illustrating a portion of a matrix array of another conventional liquid crystal display device.

[Figure 7]

A cross sectional view taken along line C-c of Figure 6.

[Reference Numerals]

1 Gate line

2 Source line

3	Pixel electrode
4	Source electrode (region)
5	Gate electrode
6	Drain electrode (region)
7	Thin film transistor
8	Light shielding film (black matrix)
9	Transparent insulating substrate
10	Polycrystalline silicon film
11	Gate insulating film
12	First interlayer insulating film
13	Second interlayer insulating film (interlayer insulating film A)
14	Third interlayer insulating film (interlayer insulating film B)